Available online www.jocpr.com

Journal of Chemical and Pharmaceutical Research, 2014, 6(10):639-645

Research Article

ISSN : 0975-7384
CODEN(USA) : JCPRC5

Using single CCD and CMOS image sensor to construction video and image acquisition system

Dongmei Li [#] and Aiju Wang [@]

[#] *Nanyang Institute of Technology, Henan Nanyang, China*
[@] *Information Engineering Institute, Zhongzhou University, Henan Zhengzhou, China*

ABSTRACT

This paper analyzes the structure and working principle of single CCD camera motion control system hardware, and the realization of the CCD camera motion control using the GEL language program. The system uses DM642 chip as the core processor, CCD camera, video decoding chip and DM642 capture video port and CMOS image sensor developed single channel real-time image and video acquisition system based. The paper presents design of video and image acquisition system based on single CCD and CMOS image sensor. Experimental verification of the combination are tested on the prototype system, the test results achieve the desired design goals.

Keywords: Single CCD, CMOS Image Sensor, Video and image acquisition.

INTRODUCTION

Stereo vision was directly simulated scene processing of human vision, stereo information can be measured scenes flexibly in various conditions, its role is not to replace other computer vision method, and it is the research on it both from the visual angle and in engineering application is of great significance.

CCD image sensor consists of a photodiode arranged two dimensionally and transfer circuit on silicon substrate [1]. The photodiode converts light into electric charge, followed by conversion circuit transfer and output. CCD image sensor according to the delivery methods are divided into two categories (Figure 1). Interline transfer (IT) almost every pixel has a shift register, and the image from the photodiode value to the shift register. The micro mirror covered with CCD, in order to improve the duty factor. In the frame interline transfer (FIT) CCD (known as the full frame transfer CCD), CCD image data to a whole frame into the serial shift register, which is not processing of the original image.

In the computer vision system, stereo vision (or binocular vision) are two the same performance, fixed position relative to the CCD camera, two images to obtain the same scene depth information, calculate the space on the two images to determine the parallax of the scene, and the 3-D shape and location of the computer reconstruction the surrounding scenery. Binocular vision and human visual perception process is similar, it is modeled after the human use of method of binocular visual cue perception distance, to realize 3D information perception, therefore the binocular vision in the visual field is very active.

Binocular vision system requirements gathering two video images at the same time, the synchronization problem hence there must be a dual channel video signal. Design of the high speed fusion system CCD camera image according to the actual application is allowed by the external synchronization signal to trigger the synchronization to solve the synchronization problem of dual channel video signal in the system, namely the synchronous signal extracted from the video signal output in the long wave infrared imaging instrument, to work the imaging system

synchronous CCD channel, achieve two input video signal synchronization purposes.

Small power CMOS devices, the mobile internet terminal developers and manufacturers are very attractive. Competition, forcing CCD manufacturers stepped up to product improvement. Some focus on the mobile phone market makers are racing to develop small and low power CCD camera module, super image quality others focus on the CCD sensor.

Research on single CCD video acquisition and motion control is based on DM642. RS-232 communication protocol of DM642 based on EVM, and it is to study and analyze the single CCD camera motion control system's hardware composition and working principle. Methods the task function uses the GEL language program and control CCD movement combining, and displayed in real time video acquisition of single channel at the same time, using the keyboard to control the EVI-D100P color CCD camera in the range of eight dimensional space motion, and the experimental results of single CCD motion control system is given. The paper presents design of video and image acquisition system based on single CCD and CMOS image sensor.

2. Development of video and image acquisition system based on single CCD

Motion control of a single CCD camera is an important part of binocular vision system. This paper first introduces the hardware structure of DM642 motion control system based on single CCD; then gives the task requirements of single CCD motion control and design.

Image storage unit mainly consists of static memory SRAM, real-time image data stored in the output image forming unit, for computer acquisition, processing image data. The image data acquisition unit is mainly composed of data acquisition card and data acquisition interface circuit completed the acquisition of image data on image storage unit stores the job. The system software is developed using VC++, complete control of the hardware circuit and the image data acquisition unit to process and display, to reproduce the imaging unit capture graph.

The CCD image sensor, charge coupled device camera; CCD replace silicon target camera is an important turning point in the history of the development of machine vision. The CCD camera is based on CCD chip as the core, the natural physical image after photoelectric conversion, a video image signal. At present, the machine vision system, the CCD camera with its small volume, reliable performance, and high resolution has been widely used.

In addition to the resolution and image sensor camera quality, size is also very important for the mobile phone market. Compact optical format 1/4 inch or smaller is the key design requirements for mainstream handheld devices. The new pixel technology has been able to achieve 1.75 micron pixel, and can keep the realization of the 3000000 pixel resolution using 8x8mm format under the condition of excellent quality, as is shown by equation1.

$$C_c(\tau,t) = X(t-\frac{\tau}{2})X^*(t+\frac{\tau}{2}) \quad (1)$$

EVI-D100P color CCD camera using the standard RS-232 serial port to achieve accurate positioning can rotate around and a full range of electric head pitch. Its input / output control interface parameters are as follows: RS-232C standard, 8 core micro interface, the baud rate of 9850bps, 9 data bits, no parity, 1 start bit, 1 stop bit.

In the point wise successively read each pixel signal and noise components at the same time, eliminate the fixed pattern noise transistor characteristics caused by the unbalanced in the same circuit, which is used to eliminate the hard line. In order to eliminate the fixed pattern noise and dark current caused by, also from HAD CCD. Whole accumulation layer is formed on the sensor surface; thereby inhibiting the dark current is not caused by incident light. To reduce these two kinds of fixed pattern noise, the S/N ratio increased 25 times, the high quality of CMOS image sensor.

The output video signal of CCD in addition to the image signal useful also includes a high DC component and noise [2]. If not treated, will seriously affect the quality of image sensor, and it is so the CCD noise of video signal processing is very important. CCD video signal processing purpose is as far as possible to eliminate all kinds of noise and interference, but not loss of image detail; and that in the dynamic range of CCD image signal with the target brightness changes linearly, and at the same time, in order to facilitate computer processing and mass storage, also must make the digitized processing of the CCD output signal.

The communication protocol of EVI-D100P color CCD camera with RS-232C standard, the specific requirements of EVI-D100P type CCD camera communication protocol: transmitter (the system that DM642) address is fixed at 0;

the receiver (CCD camera) address is 1 - 7, used to set the EVI-D100P address; the baud rate is 9600bps; 8 bits of data; 1 start; 1 stop; no parity; the highest effective bit MSB (Most Significant Bit) the first transmission, as is shown by figure1.

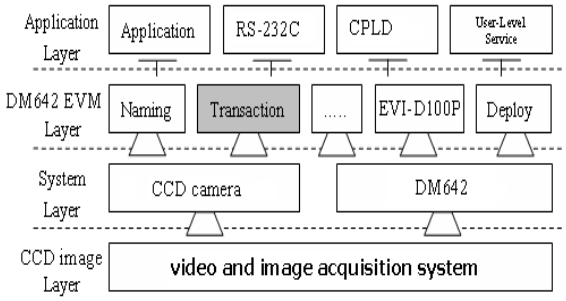

Fig. 1. Development of video and image acquisition system based on single CCD

The strict requirements of occasions for power, through the programmability of CPLD will interface with the ARM timing part of the interrupt port, only bus combinational logic is connected, can reduce the power consumption of CPLD so as to achieve the effect of scheme 1; for the collection of high speed and power requirements is not high, can give full play to CPLD advantages, to achieve recognition output image sensor synchronous signal by using combination and sequential logic, and the image data into the SRAM.

Control command of CCD camera is a basic unit in the serial communication; the basic unit is called packets, as shown in Figure 1 structure data packets. The first byte packet data is the data of Baotou, which includes the transmitter and the receiver's address, for example, the EVI-D100P address is 1, the sender address is 0, Baotou is the data is sixteen hexadecimal number 81H.

When the OV7620 work in master mode, the YUV channel it will continuously to the bus output data. If the YUV channel OV7620 is directly connected with the D15 data bus in LPC2210 ~ DO, it will interfere with the data bus, the LPC2210 can not operate normally; if you use the 74HC244 isolation method, using the data bus time, would greatly reduce the operating speed of the system, so that the LPC2210 can not be timely removed the data bus, cause the image data is not complete.

DM642 chip accesses to external memory must also be through the EMIF interface, UART-0 and UART-1 input / output control interface can be regarded as an external memory unit specific, the read and write operations must also be through the EMIF interface [3]. DM642 EMIF provides external bus width of 64 bits, 8 bit support, 16 bit, 32 bit and 64 bit data access, and EMIF can automatically complete the external access less than 64 bit data packing and unpacking processing.

$$C(t) = \frac{E[B(t), B(-t)]}{E[B(t)^2]} = 2^{2H-1} \tag{2}$$

System image acquisition order issued by the computer imaging parameters, and it is sent to the imaging unit system at the same time. Imaging parameters through the computer serial port, transmitted to the FPGA microcontroller. Start the FPGA imaging control module, imaging control module through SPI (Serial-to-Parallel Interface) bus on the image sensor LUPA-300 internal register of imaging parameters, such as exposure control, window control, and frame rate control.

In the image of the photosensitive area left, each line has 22 pixel shading screen covered by metal. These dark pixels can provide reference for the subsequent processing circuit black level image. In addition, in the image of the photosensitive area and image storage section has 4 rows of pixels are also metal shading screen covers; they are there to avoid the charge sensitive area of the leak to a storage area.

The TL16C752B chip in receiving an external device (the system EVI-D100P color CCD camera) data, complete serial to parallel conversion; after receiving DM642 data, complete the parallel to serial conversion, and serial transmission. According to the control interface parameters EVI-D100P color CCD camera input / output.

Monocular vision system is able to achieve mechanical motion function is similar to the human eye and head. Each independent movement direction is called a degree of freedom, the number of degrees of freedom; the functional

vision platform is stronger, more close to the human visual system function.

CCD is known as the "charge coupled device", CCD is actually a semiconductor electronic image from out of organized stored. CMOS is known as the "complementary metal oxide semiconductor", CMOS is actually just the transistors on silicon block technology, no more meaning. Sensor is called CMOS sensor is in order to distinguish it from the CCD sensor, has nothing to do with real image processing method and sensor.

To study and analyze the structure and working principle of single CCD camera motion control system, using UART-0 development board (J11) connected to the EVI-D100P color CCD camera, and displayed in real time video acquisition single CCD at the same time, the realization of the CCD camera motion control using the GEL language program.

In order to simultaneously control two cameras, two standard RS-232 serial ports, and the DM642 EVM development board has two such interfaces (UART-0 and UART-1) [4]. The UART-0 and UART will be the two EVI-D100P color cameras (CCD-0 and CCD-1) connected with DM642 EVM development board, and it is a synchronous motion control system of dual CCD.

3. Using CMOS Image Sensor to Design Image Acquisition System

The system achieves high frame rate digital image acquisition, display and storage. This system has been successfully applied in a military range measurement, the project is expected to benefit more than 300 mit, the source of data simulation analysis and experiment on the system verification, and by using the method of simulation analysis and experimental verification of the combination are tested on the prototype system, the test results achieve the desired design goals.

Image acquisition system mainly consists of a CMOS image sensor, DSP and processing circuit. The concrete scheme is when the CMOS image sensor is configured to receive signal acquisition, start, start the image collection, and the collected image information into the DSP image format, for behind the conversion, processing and display ready. DSP image data of the CMOS image sensor to capture the stored in the off chip memory SDRAM, for processing, and according to the requirements of image recognition algorithm in detail, data processing, and the result is transmitted to the display on the show, as is shown by equation3.

$$E_{jB}^{\xi}(m,n) = \sum_{m'\in J, n'\in K} w_B^{\xi}(m',n')[D_{jB}^{\xi}(m+m',n+n')]^2 \tag{3}$$

After power on, first by LPC2214 through I2C bus configuration camera work state, need to configure the main output image data format, rate, whether the white balance, and automatic gain is open. After the configuration is complete, the LPC2214 signal image acquisition to the CPLD, the CPlD operation of SRAM bus, and the image data into the SRAM through the detection of the OV6620 output timing. Of course, write SRAM need to strictly comply with the timing of SRAM operation. A frame of image acquisition is completed, the CPLD set a flag to notify the LPC2214, if the LPC2214 is in the idle state, the CPLD is informed the bus use right switch to LPC2214, from LPC2214 to read the data in the SRAM and image processing.

The output waveform of CMOS image chip is ZV port format. Figure VSYNC is a vertical field synchronization signal, the falling edge represents the beginning of a frame of the image (CMOS is column image collection), HREF is the horizontal field synchronization signal, and the rising edge represents the beginning of a series of image data. PCLK is the output data synchronization signal, Y is the image gray information.

The system acquires images from the camera, calculation of the target with three pieces of DSP chip's position and velocity, the image processing results and the synchronization of the UAV attitude data is then sent to the fourth DSP chips, and finally to a real-time controller to control the UAV flight, thus completing the detection and tracking of targets[5].

Interrupt response time the speed of image acquisition is mainly limited to LPC2210, if the DMA controller with ARM chip, and has higher processing speed, can greatly improve the speed of image acquisition system. For example, with the ARM9 kernel S3C2410, the highest frequency of 203 MHz, a DMA delivery time is about 30 ns. Period is less than the default PCLK 74 ns; image acquisition speed can achieve 30 fps.

CMOS camera chip is with micron MT9V011. The maximum output rate of MT9V011 images at 30 frames per second, and the LPC2104 processor I/O port to read and write speed is far from enough, the loop will one I/O its mouth is set high and then immediately set low, output of the Fang Bo frequency is less than 4MHz. The data of

image data with respect to the resource limited embedded system is too large, the size of an image output data is MT9V011 by default to 300K bytes, and LPC2104 processor memory size is only 16K bytes, as is shown by figure2.

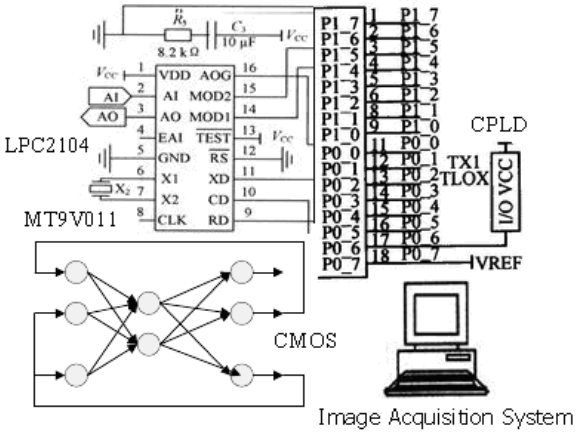

Fig. 2. CMOS Image Sensor to Design Image Acquisition System

Single chip solution due to external components and interconnects with less number of advantages in the same solution talent showing itself, these advantages for small diameter endoscope has a very important significance. High integration is synonymous with low cost, CMOS image sensor has been favored by endoscope application of various types [6]. Because of lower power consumption, manufacturing CMOS image sensor is suitable for autonomous miniature camera, the camera can be mounted on the pill the size of the box, and the data can be wirelessly transmitted to the receiving station.

CMOS image acquisition chip system using IBIS5-A-1300 COMS image sensor chip, a resolution of 1280 * 1024, full frame acquisition rate up to 27fps, maximum dynamic range up to 100dB, 6.7 m × 6.7 m high fill factor pixel, filling coefficient of 66%, support the rolling shutter and synchronous shutter two shutter mode. The internal integration of the output amplifier can adjust the gain and bias, and 40Msamples/s high speed A/D conversion module, A/D quantization levels for the 10bit, can be directly output analog signals or digital signals, internal registers and the controller can adjust the real amount, the sensor working state. Chip support window technology sub sampling technique based on real-time frame rate, improve the actual need.

Corresponding to the internal registers of the CMOS image sensor address, the first 12 (bit<11:0>) as the data bit, imaging parameters corresponding to the system imaging unit [7]. When the imaging parameters set, imaging parameters LUPA-300 read the internal registers, and the FPGA imaging control module sends driving time to the image sensor, image acquisition. LUPA-300 as image sensor system, sampling and quantization image its interior will be acquired, digital image output in the control of external logic, also sends out the column effective LINE_VALID and frame valid FRAME_VALID signal, to facilitate effective digital image data acquisition.

In this paper, by adding the CMOS digital image sensor in the embedded processor system a low-end, and the preparation of hardware description language program, embedded processor program, realized the acquisition of image features.

4. Design of Video and Image Acquisition System based on Single CCD and CMOS Image Sensor

The system uses DM642 chip as the core processor, using CCD camera (CCD-0), video decoding chip (SAA7115-0) and DM642 capture video port (VP0) composed of real time video acquisition system of single channel; single CCD camera (CCD-0) of the motion control system is composed of EMIF interface, DM642 two-way double buffered serial port (TL16C752B chip), level conversion chip (MAX3243-0), universal asynchronous serial interface (UART-0).

CCD image sensor, technical parameters and characteristics are different, but all the larger pixel (6.5, 12 μ m2), the system comes with refrigeration, resolution of 12 ~ 16 bit low readout noise and low dark current. For example, SPOT Persuit, Xplorer index were lower than room temperature 33 □, 71 □, both the dark current is 10 times (0.022, 0.002e / pix• s), 21.4 mm CCD, 10.4 μ m × 10.4 μ M / pixel, 2048 x 2048 pixels, full well 30000e, 14 bit resolution basic and dark current and readout nois.

Progressive video CMOS imaging sensor can output 30f/s VGA size, and the television shows the need for 50f/s (PAL) or 60f/s (NTSC system) of the interlaced video image. In order to solve the frame rate mismatch problem, the control chip needs to embed adaptive frame rate control module and an on-chip memory in order to obtain a smooth video streaming. However, unless absolutely necessary, large capacity on-chip memory should be avoided, because generally speaking, it will increase the area of the chip and reduce the IC yield. The common image compression technology, such as JPEG or ADPCM, can further reduce the internal frame memory capacity requirements.

If the CCD work in low light conditions, even if the signal gain is big, under the reference voltage through the voltage video signal processed may still be less than ADC, so the output video image distortion. In order to improve the gray resolution under low light conditions, need to make dark refer to reference voltage level higher than the ADC of the output video signal, then just adjust the gain is not enough, also need to offset the video output signal to adjust. The bias adjusted XRD4460 is also through the serial programming control on-chip 8 bit offset register. Set the bias power up default value 08H, offset adjustment range is from 02H to 08H.

The serial communication protocol chip TL16C752B as follows: set the baud rate of 9600bps, 8 data bits, no parity, 1 start bit, 1 stop bit. For the realization of serial communication settings of the TL16C752B chip register as shown in table 3-4 (two UART TL16C752B chip port register are exactly the same, so the table is only a group of UART port register listed in 3-4). Because the TL167C52B chip has two identical UART port register, so as to use the UART-0 port of the single CCD motion control system, only in accordance with the serial communication protocol EVI-D100P CCD color video camera, a group of UART corresponding to the UART-0 mouth of register, as is shown by equation4.

$$\Psi(m,s) := [\overbrace{0,\cdots,0}^{s-1}, C((m-1)M+s), \overbrace{0,\cdots,0}^{M-s}] \tag{4}$$

Economic operation of portable equipment has nothing to do with the power network only have in the components and subsystems will work with low power requirements. Obviously, the CMOS technology has advantage in this respect, because the CMOS image sensor is designated for low supply voltage alone (3.3V or 2.5V), and most of the CCD chip power supply voltage is needed by multiple and higher values (for example: 12V). The voltage transformer must be used to consume energy and take up valuable space on the circuit board to generate.

In the single CCD motion control system, the development board TL167C52B doubles buffering double UART chip driver buffer by RS-232 (MAX3243-0), sent to the UART-0 connector type DB-9 (J11), so as to realize the serial communication with CCD camera. I/O power DM642 chip 3.3 V, and serial communication interface signal logic "1": -3V-15V, logic "0": 3V15V. Therefore, in order to realize the serial communication of DM642 chip and the CCD camera must first go through the interface level matching.

The ranks of addressing are functions of CMOS device are similar to DRAM, can provide the degree of attention window, and support the electronic chip pan, tilt and zoom. These functions can be the need for image compression, motion detection and object tracking provides more flexibility. Addressing the characteristics of flexible and high speed CMOS combined with auto focus and auto exposure provides numerous options for designers to improve. CMOS products using the manufacturing process based on DRAM can provide sufficient preparation time, yield, productivity and the expected advantages.

Control method of free switch dual channel using the GEL program, combined with the task function here GEL program and control the CCD direction moving phase method, and displayed in real time video acquisition of single channel at the same time, the eight directional motion using keyboard to control the CCD camera in the three-dimensional space. In this paper, the GEL language program is loaded, the CCD used to control movement of the dialog box as shown in figure 3.

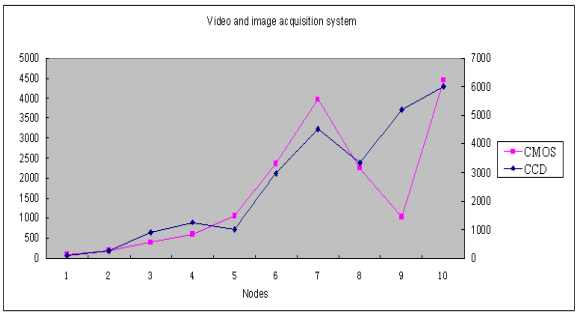

Fig. 3. Compare of video and image acquisition system based on single CCD with CMOS image sensor diagram

The experimental results show that: the RS-232 communication protocol based on DM642, this paper implements the single CCD camera's range of motion control, to control the mission system requirement, laid the foundation for the further study of synchronous motion system of dual CCD camera control. Low power high level RS-232 standard conversion chip MAX3243 to realize the conversion between CMOS logic level and UART logic level, is a multi channel RS-232 line driver / receiver, the maximum transmission data rate of output of the device is up to 250kbit/s and 30V/us, so the level conversion chip can ensure the mixed logic level conversion rate meet the system requirements.

CONCLUSION

The paper presents design of video and image acquisition system based on single CCD and CMOS image sensor. In the course of the experiment, the DM642 EVM development platform is placed in the computer desk on the laboratory. Single channel video acquisition system and display in real time collection at the same time, represented by keyboard input defined the corresponding control function of digital and execution, the system call the corresponding code, so as to control the CCD camera as the corresponding action. From the CCD camera and the display screen faces a single CCD motion control experimental results are shooting.

REFERENCES

[1]. Zhang X; Wakamatsu H. *Journal of the Robotics Society of Japan*, **2002**, 20 (1), 89-97.
[2]. Lina Gao; XiaoDong Hu. *AISS*, **2012**, 4(20), 318 - 325.
[3]. Li Xinwu. *Journal of Chemical and Pharmaceutical Research*, **2013**, 5(12), 113-117.
[4]. Vallerand Steve; Kanbara Masayuki; Yokoya Naokazu. Binocular Vision-Based Augmented Reality System With An Increased Registration Depth Using Dynamic Correction Of Feature Positions. Proceedings Of the **2003** IEEE. *Virtual Reality*. March, **2003**. 22, 271-272.
[5]. Xiaoke Wei; Zuqiang Wang; Hui Xu. *AISS*, **2012**, 4(22), 99 -105.
[6] Preeti Srivastava. *Journal of Chemical and Pharmaceutical Research*, **2014**, 6(1), 570-579.
[7]. Likun Tian; Xiaohong Liu; Jie Li; Xiaoguang Guo. *JDCTA*, **2012**, 6(20), 130-139.