Development of intelligent traffic control system based on FPGA and single chip microcomputer technology

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ABSTRACT

There are a large number of combinatorial logic resources in FPGA, can complete the design of combinational logic circuit, larger scale. Microcontroller design of intelligent traffic light control system, change of state control signal by SCM, basically can be specific traffic directing traffic. Intelligent transportation system is a general term of various high-tech field of transportation system. The paper presents development of intelligent traffic control system based on FPGA and single chip microcomputer technology. Finally, experiments show the efficiency of the design of the intelligent transportation system.

Keywords: Intelligent transportation system, FPGA, single chip microcomputer.

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INTRODUCTION

Traffic control system is a modern society with a unique set of public management system of logistics, transportation and other transportation development. To ensure safe and efficient traffic order, except for a series of traffic rules, must also be achieved through certain technical means. Modern science and technology, especially the technology problem solving system electronic science and technology development and mature and can better build in hardware and software requirements. At present, the study of traffic control can realize the automatic intelligent completely, even the whole regional integration into a unified system, can automatically adjust according to the specific scientific normal time and burst periods.

Intelligent transportation system is a general term of various high-tech field of transportation system [1]. All aims at the application of component technology means, to improve traffic conditions, traffic problems in a variety of technical system.

The goal and function of ITS includes the following aspects: to improve the safety level of traffic; congestion; keep the traffic smooth; improve the transport network capacity; to help people in the use of more safe, convenient traffic, fast, comfortable; reduce the pollution degree to the environment of transportation and energy saving; improve the transportation efficiency of production and economic benefit. To improve the transport level with the traditional means of comparison, infrastructure, ITS is not simply rely on to build more consume a lot of resources to achieve the above goal and function, but in the existing or perfect infrastructure, rely on advanced science and technology, the integrated use of multi-disciplinary knowledge to achieve its objectives and functions.

2. FPGA design flow and SCM traffic control

The FPGA/CPLD chip is a ASIC chip special features, in addition to ASIC, also has the following advantages: with the VLSI (VLSI) constantly improve the technology of single chip can contain millions of transistors in a chip, FPGA/CPLD is also increasing, the monolithic gate count has reached millions of gates, it the realization of the function is also more and more strong, but also can realize system integration, system on a chip SOC.

The FPGA development system includes two parts of software and hardware. System software development refers to the special programming language and the corresponding assembler or compiler. The development of the hardware of the system includes a computer and programmer [2]. The programmer is a special device write and erases the FPGA, can provide the power supply voltage and the control signal required for write or erase operations, and through the serial interface to receive programming data from the computer, the final written into FPGA.

$$x(t) = \text{Re}\left[\sum_{i=1}^{n} a_{C_i}(t) \exp\left(j \int \omega_{C_i}(t) dt\right)\right] \tag{1}$$

Using the FPGA based method has the advantages of short period, the use of flexible, easy to modify and obvious advantages. But, with the development of the FPGA device, the design language and the development of electronic design automation tools and improved, more and more electronic systems to design using FPGA. Future use of FPGA device design products will appear in various fields. Therefore, the traffic light controller design scheme based on FPGA to achieve the required function.

The traffic light system is composed of four parts: vehicle detection circuit, signal circuit, time display circuit, an emergency switch. According to the road traffic congestion, traffic jam of the crossing using single-chip microcomputer control technology is presented and design scheme of software and hardware two improvements. 1, according to the road intersection traffic flow automatic regulating access time. 2, consider the special vehicle traffic conditions, the design of emergency switch.

Single-chip design of the traffic light control system, change of state control signal by SCM, basically can be accepted, directing traffic, of course, access to the LED digital tube can display the countdown to remind users, more humane [3]. Based on this system, joined the violation detection circuit and the vehicle flow detection circuit for single chip microcomputer data acquisition, the specific treatment, timely adjustment of the control, in order to transcend the limitations of visual command, at the same time, the buzzer, in the hearing to command reminder.

3. Development of intelligent traffic control system based on FPGA and single chip microcomputer technology

Intelligent transportation system is an advanced integrated traffic management system. In this system, the vehicle on its own intellectual freedom on the road, the road on its own intelligent traffic flow is adjusted to the best state, with the help of the system, management of the road, vehicles will have be crystal clear. City traffic management traditional basic is spontaneous, each driver judge according to their own choice of routes, traffic signal signs only play a guiding role in static, limited.

The architecture of ITS is a subsystem, system which contains the interrelationship between the sub-systems and integrated mode, and each subsystem in order to realize customer service function, should have to meet the user's demand function. According to the definition, the ITS system structure determines how the system structure, the communication protocol between the function module and the module and interface design, its design must include the implementation of customer service function of all subsystems.

FPGA Compiler II is a perfect FPGA logic analysis, synthesis and optimization tool, it from the HDL form is not optimized netlist generated netlist optimization, including analysis, synthesis and optimization of three steps. The analysis of HDL syntax rules, is using the Synopsys standard for HDL source files to analyze and correct grammatical errors; synthesis is based on the FPGA structure and the device is selected as the goal, to HDL and FPGA netlist of logic synthesis; and the optimization is based on user's logic optimization design constraints on speed and area, FPGA the net list file generating an optimized, for FPGA placement and routing tools, the circuit optimization in manufacturer specific component library, independent of silicon holding, but can be driven by constraints.

$$\phi(t) = \sqrt{2} \sum_i h(k) \phi(2t - i) \tag{2}$$

This system takes the MCU as a core, consisting of a set of traffic flow collection, processing, automatic control for closed loop of a control system. System hardware circuit is composed of vehicle flow detection circuit, MCU, violation detection circuit, light, LED display, button, a buzzer.

Intelligent traffic signal was installed can display a green light, red light display circuit waiting time, the use of digital tube display circuit is a very good method. Due to the west to the East and west to east to display the same

time, show the south to north direction and north south direction of the same time, we only need to consider the four digital tube display circuit, wherein the two north-south east-west direction, two.

VHDL is mainly used to describe the structure, behavior and function of digital system, the program structure is characterized in that a circuit or a system into port and internal function algorithm to achieve the two parts. For a circuit module or digital system, defines the external port, once the internal function algorithm is completed, other system can be directly according to the external port calls the circuit module or digital system, without having to know the internal structure and algorithm.

$$L = \sum_{i=1}^{c} \sum_{k=1}^{n} \mu_{ik} \ d_{ik}^2 \qquad\qquad (3)$$

Reset input. When the oscillator, the RST pin for two machine cycles of high level will make the MCU reset. WDT spillover will enable the pin outputs high level; set the SFR AUXR DISRT0 (address 8EH) can open or close the function. DISRT0 defaults to RESET to output the high level open.

UINA will transport system into 3 layers: transport layer, communication layer and system layer. Transport layer performs the function of transportation, communication layer in order to provide communication service between transport layer connection of components, system level reflects the relationship between researchers, policy planners and other ITS users [4]. To determine the physical structure of the factors to consider system, but the system layer does not belong to the physical structure, but described in the implementation strategy. The physical structure of the transport layer and the communication layer are described.

$$u'(x_1, x_2) = \sum_{s=-n}^{n} \sum_{t=-n}^{n} w(s,t)u(x_1 + s, x_2 + t) \qquad\qquad (4)$$

Intercity intelligent transportation, in the intercity traffic, accompanied by Chinese expressway investment scale continues to expand, increasing construction mileage, highway management required for the traffic engineering facilities, especially the communication, monitoring and charging system will continue to expand the demand of highway. Intelligent transport system is the use of information technology, data communication transmission technology, electronic sensor technology, control technology and computer technology and traffic engineering technology based comprehensive, integrated system, mainly by the monitoring system, communication system and charging system three parts.

The FPGA/CPLD integrated development environment, Altera is the world's largest supplier of programmable logic device. Max+plus Ⅱ friendly interface, easy to use, known as the industry's most easy to learn the EDA software. Max+plus II can complete design input, component adaptation, timing simulation and functional simulation, programming to download the entire process, it provides an architecture independent design environment, designers can easily design input, fast processing and device programming.

The program is compiled by using MAX+PLUS II software, to generate the simulation timing analysis and downloaded to the relevant documents of programmable devices.
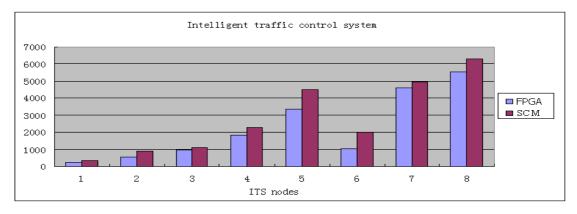

Fig. 1. Development of intelligent traffic control system based on FPGA and single chip microcomputer technology

Intelligent traffic control system here using AT89S51 microcontroller as the core of the system hardware design, including: input traffic, a key state and violation detection sensor signal; output to control the traffic signal lights off state and time, as well as the LED digital countdown display tube, as is shown by figure1.

The structure of hardware platform once identified the function framework in the form. Building on the hardware platform, and it is control and coordination of each part of hardware. The system function is implemented by software and hardware, the scalability of the system software, the functions may be strong to weak, may be much difference. The software adopts C# language, not only easy to program and debug software, can also reduce the failure rate and improve the reliability of software. The simulation includes the function simulation, timing simulation and timing analysis, to verify the logic function design project is correct by using the simulation software.

CONCLUSION

Users can repeatedly programming, erase, or in the peripheral circuit without moving with different software can realize different functions. FPGA/CPLD software package in the various input tools and simulation tools, products and layout tools and logic, circuit designers in a very short period of time can complete the circuit input, compilation, optimization, simulation, production until the final chip. When the circuit has a small change, it can show the advantages of FPGA/CPLD.

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