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Application of FPGA in high-speed CMOS digital image acquisition and color recognition system

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ABSTRACT

FPGA can solve the lack of custom circuit, and overcome the original programmable gate device limited number of faults. The paper presents application of FPGA in high-speed CMOS digital image acquisition and color recognition system. Color recognition system is mainly composed of analog and digital two parts. The analog part mainly used photoelectric signal conversion, amplification and filtering the noise signal. The digital part is mainly used for digital signal in the sampling of the A / D median filter, check the log table, logarithm ratio, and the display operation. High frame rate CMOS imaging unit mainly consists of a CMOS image sensor and control chip FPGA, it is the imaging system components, using the image to capture fast moving objects, the circuit output for digital image data. This paper describes the SCCB bus configuration method and image acquisition part of the structure.

Keywords: CMOS image sensor; FPGA; Color recognition; Image acquisition.

INTRODUCTION

Video image acquisition is the front portion of the video signal processing system, is developing to high speed, high resolution, high integration, high reliability. Image acquisition system is widely applied in the industrial, military, medical and other fields, such as used in remote monitoring, security, remote meter reading, video phone, industrial control, pattern recognition, medical equipment and other fields have a wide range of applications. This paper introduces a kind of image acquisition system based on FPGA, the user can according to need logic module and I/O module of the FPGA internal reconfiguration, the reconfiguration system; and the use of this design, convenient design errors found in a timely manner, can effectively shorten the development time, improve work efficiency.

CMOS (Complementary Metal Oxide Semiconductor) image sensor is a new sensor developed in recent years, compared to the CCD (Charged Coupled Device) and other solid sensor; it has small volume, light weight, high integration, low power consumption, low cost, easy programming, easy control and high speed capture. Especially in recent years, with the continuous improvement of the development of submicron and deep submicron process technology and device structure, the image quality of the image quality of CMOS image sensor has been close to or reached the CCD image sensor. Based on the above features, CMOS image sensor is suitable for high frame rate image acquisition system.

High speed digital image acquisition system is an effective tool to study physical phenomena happen instantly, obtain the high-speed movement of objects in digital image, is based on the study of physical phenomena happened in an instant [1]. The high speed image acquisition system (generally refers to the frame rate is more than 100fps) is mainly used in military field. The CMOS sensor uses CMOS technology semiconductor circuit is the most commonly used, can easily be peripheral circuit (such as AGC, CDS, Timing, generator, or DSP) is integrated into the sensor chip, so it can save the periphery chip cost; in addition, because the data in CCD by charge transfer way, as long as there is a a pixel cannot run, will lead to a whole row of data cannot be transmitted, so CCD control sensors yield many more than the CMOS sensor is difficult, even experienced manufacturer also is very difficult in

the products of the half a year to break through the 50% level, therefore, the cost will be higher than the CCD sensor, CMOS sensor.

Color recognition system is mainly composed of analog and digital two parts. The analog part mainly used photoelectric signal conversion, amplification and filtering the noise signal. The digital part is mainly used for digital signal in the sampling of the A / D median filter, check the log table, logarithm ratio, and the display operation. As a special integrated circuit (ASIC) is a semi-custom circuit in the field, FPGA can solve the lack of custom circuit, and overcome the original programmable gate device limited number of faults. It is no exaggeration to say, FPGA can perform any function of digital devices, high-performance CPU, down to 74 simple circuits, can be achieved by FPGA.

Therefore, FPGA can be used repeatedly. FPGA programming does not have a dedicated FPGA programming, using generic EPROM, PROM programming device only. When it needs to modify functional FPGA and EPROM can only change. In this way, the same FPGA, different programming data, can produce different circuit functions can. Therefore, the use of FPGA is very flexible. Can say, the FPGA chip is one of the best choices for small batch system to improve the integration, the reliability of the system. The paper presents application of FPGA in high-speed CMOS digital image acquisition and color recognition system.

2. CMOS Image Sensor Data Acquisition System based on FPGA

CMOS sensor is one of the widely used image sensor, is a photoelectric conversion by the photosensitive diode, the image is converted into digital data. In the CMOS sensors, each pixel is adjacent to an amplifier and A/D conversion circuit, memory circuit in a similar manner to spins out of data; it is suitable for mass production, suitable for small size, low price, and high quality requirements of the application of no camera. With the development of technology, CMOS image sensor is high sensitivity, high resolution, high dynamic range, integration, digital, intelligent "camera on a chip" solution direction.

A simple rule is the microcontroller using FPGA instead of the standard can not produce a cost-saving alternative. Not only through the micro controller integrated peripherals to satisfy the boundary conditions, FPGA solutions can become more attractive, such as the PWM and the number of channels, counter / timer or I/O port number.

With the development of integrated circuits, large-scale programmable logic device widely used in the field of circuit design, it has low power consumption, high reliability, and greatly reduces the size of circuit boards. The internal structure of FPGA determines the superiority of FPGA in the sequential design aspects. This design uses FPGA chip XC3$50 as the hardware design platform [2]. Virtex II FPGA architecture based on nm technology, using 90, 8 layers of metal technology, embedded hard multiplier and digital clock management module. From a structural point of view, it would be logical, memory, arithmetic, digital processor, I/O and system management resources perfectly together, so that it has a higher level application, more widely.

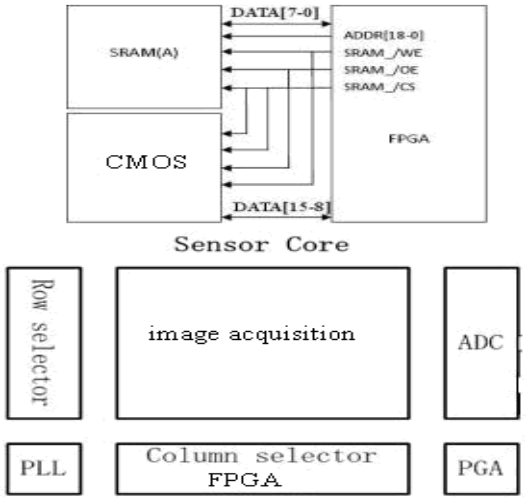

Fig. 1. CMOS Image Sensor Data Acquisition System based on FPGA

The I2C slave device (slave), GPIO, memory, DMA and user special components, such as the port monitor to start the memory transfer. MSB provides for "shared bus" or "Slave Side-Arbitration" configuration of the functions of the device, which means that the automatic generation of arbitration in the right form. The combination of these

elements in the MSB, the use of this method in a few minutes you can generate FPGA code. Then in the Mico32, you can write C code, using the provided debugging check. All components are easily reused.

Parallel operation of FPGA internal procedures, have to deal with more complex functions: the ability to program are executed serially, executed a to perform the next, in dealing with emergencies can be invoked only limited interrupt resources; and FPGA different logic can be executed in parallel, can handle different tasks at the same time, which leads to more FPGA efficiency.

CMOS image sensor based on charge pump, using a simple charge pump up the reset pulse signal amplitude, the charging voltage in the pixel unit to supply voltage; parameter adjustment the source follower, expand the node voltage in the lower bound charge integral cycle swing range, the two kinds of scheme can effectively improve the charging voltage swing, thereby improving the dynamic range of the sensor. The reset pulse signal amplitude increases and decreases the time constant charging; shorten charging time, which can improve the image acquisition frame rate.

For visible light into electrical signals according to the basic technology, image sensor can be divided into two categories. They are CCD (charge coupled device) sensor and CMOS (complementary metal oxide semiconductor) sensor [3]. So far, the shipment of image sensor volume is the largest CMOS sensor. This paper focus on the CMOS sensor interface, as is shown by equation1.

$$\sum h(n)h(n+2k)=\delta_{k,0} \tag{1}$$

Research on the visual system has become a hot spot, also has the developed system can be used for reference. But most of these systems are based on the PC, because of the complexity of algorithm and hardware structure and its application in embedded system is limited. The system of image data acquisition, image processing algorithm is implemented on the PC machine. With the development of embedded microprocessor technology, 32 bit ARM processor system has very high computing speed and strong signal processing ability, as a visual system processor; replace the PC machine to realize visual processing algorithm is simple.

The three basic types of digital electronic devices in the field: storage device, microprocessor and logic device. The logic device can be divided into two categories, namely fixed logic devices and programmable logic devices. Fixed logic devices in the circuit is permanent, for the completion of one or a set of functions. In programmable logic devices, can at any time to modify the device, to complete various functions. Two main types of programmable logic devices are: field programmable gate array (FPGA) and complex programmable logic device (CPLD), compared with CPLD, FPGA can provide the logic density, higher characteristic more and higher performance.

Image acquisition mode CMOS sensor is active, the charge generated by the photodiode will magnify the output directly by the transistor, but the CCD sensor is a passive collection, additional voltage to charge mobile in every pixel, and the applied voltage is usually needed to reach 12~18V; because of this, the CCD sensor in addition to the more high in power management circuit design in addition to the difficulty (need of additional power IC), high driving voltage for its power consumption is much higher than the CMOS sensor level.

As we see, we have a CMOS image sensor CMOS sensor suppliers such as Aptina, OmniVision launched a new built-in ISP single chip products, and constantly improve its function, extend its applications. Has introduced this kind of single chip products in addition includes exposure control, gamma correction, white balance, color saturation adjustment and gray control a variety of image processing functions, can also provide low light performance excellent, in night vision environment also has a near infrared sound excellent performance, can provide more perfect automatic white balance and automatic exposure function for the camera manufacturer, image performance favorably [4]. A series of excellent properties make it have been photographed by mobile phone, digital camera, digital camera originally applied to the progressive development of network camera, camera and other new against product areas, the expansion trend continues, is spreading, as is shown by equation2.

$$r_f = u_f u^*(n)=\begin{bmatrix} r^*(1) \\ r^*(2) \\ \vdots \\ r^*(M) \end{bmatrix}=\begin{bmatrix} r(-1) \\ r(-2) \\ \vdots \\ r(-M) \end{bmatrix} \tag{2}$$

In hardware design, all bus is connected with the CPLD; in software design, different modules separately at the function encapsulation. This with the CPLD as the center, the other device can be replaced without the need for changes to the CPLD part of the program, to the function of the system upgrade. As an application of this system, the development of the visual tracking procedures can be on the target and background color contrast between the strong cases for object tracking. Through the real-time processing of CMOS camera data, calculate the centroid coordinates of the object being tracked according to the color of the object. The following describes the function of each part of the system.

This reference design uses HiSPi serial interface in the input, output end connected to the Aptina sensor in TI TMS320DM3X5. Evaluate hardware have been tested with A-1000 sensor MT9M034/MTM024 and MT9J003 Aptina. This reference design support group (Packetized) and Streaming SP HiSPi format: 1-4 channel running at speeds of up to 700Mbps per channel. It also simulates parallel sensor output; the output bus width is 8, 10, 12, 14 or 16. It can be configured as 1.8V, 2.5V or 3.3V LVCMOS interface level parallelism.

$$fresp(x, y) = Det(Z) - kTrace^2(Z) \tag{3}$$

The image sensor, small size, low operating voltage, provides all the functionality of monolithic VGA camera and image processor. Controlled via the SCCB bus, can various resolution output frames, sub sampling, take the window way of data 8. The product VGA images up to 30 frames per second. The user can fully control the image quality, data format and transmission mode. All image processing functions including Gama curve, white balance, saturation, color can be programmed via the SCCB interface.

The image data of the system includes OV7670 data acquisition board, FPGA receive buffer plate, two pieces of SRAM cache and the system external interface [5]. OV7670 image data acquisition board is mainly to complete the image data acquisition, image data, image data bus clock, frame synchronization signal, synchronization signal and FPGA image data receiving buffer plate is connected, the FPGA coordinates two SRAM "Ping-Pong mode" read and write operations, and the completion of the external interface module.

For the high pixel 3.2M camera mobile phone, Raw Data scheme from the angle of system design is reasonable. High pixel camera mobile phone in order to replace the traditional digital camera, the image quality has reached the requirements of the professional requirements. To improve the performance of image acquisition front-end and back-end complex, image processing technology is also essential. To have the function of complex ISP integrated into the sensor, almost difficult to achieve, such as color interpolation algorithm of complex requirements to preserve a frame of Raw Data, requires a lot of buffer, do not be sensor; and increasingly high performance multimedia processor, whether processing capability, or with buffer, are very suitable for to complete this function. From the structure and performance of the whole system, this scheme is the most competitive.

Video data has its own characteristics. In different color space, representation of each component is usually 8 pixel width. Blackfin 4 video arithmetic unit and video pixel instruction set computing speed greatly accelerated video. A video pixel operation instruction can complete 4 video data component addition, subtraction, addition and subtraction mixing, average or subtraction and absolute value of 11 kinds of video pixel operation in a cycle. A large variety of applications loopfilter algorithm analysis and intelligent video moving these operations in encoding and decoding algorithm, the estimation, as is shown by equation4.

$$\psi_{a,b}(t) = \frac{1}{\sqrt{|a|}}\psi\left(\frac{t-a}{b}\right) \tag{4}$$

For dual CPU shared SRAM can be solved by reasonable connection mode. Taking into account the programmability of CPLD, the OV6620 data bus, the address of the LPC2214, data bus and SRAM bus are connected to the CPLD. Through programming to control between buses, as long as the guarantee of mutual exclusion of bus in the software, which has only one controller at the same time (CPLD or LPC2214) bus to SRAM operation, can effectively avoid the bus conflict. In this way, the hardware arbitration can be ensured by the software, the process can be achieved through the preparation of a multi-channel data selector in CPLD.

With a complete LVDS document support LatticeXP2 non-volatile FPGA series has proved to solve the electrical demand of image Sensor Bridge. The integration of PLL, I/O and gearing logic dedicated clock edge is to solve the high-speed serial interface of the sensor [6]. Finally, Ledith semiconductor (Lattice) XP2 provides a cost-effective 8 × 8mm area. In addition, because of its non characteristic volatile, LatticeXP2 series devices without external guide PROM, which further saves space on the circuit board, which makes them sensor interface attractive programmable

logic platform.

CCD sensor charge every pixel in each row will be transmitted to the next pixel, the bottom end portion of the output, and then through the edge sensor amplifier for amplifying the output: while in the COMS sensors, each pixel is adjacent to an amplifier and A/D conversion circuit, memory circuit in a similar the data output. Causes of the differences: the special process of CCD can be guaranteed not to distortion in the transmission, therefore the pixel data can be collected to the edge and then amplifying treatment; COMS process data will produce noise in the transmission distance is long, therefore must first be amplified, then integrate each pixel data.

$$E\left\{v_i(kT_i), v_j^T(lT_j)\right\} = R_i(kT_i)\delta_{ij}\delta_{kl}, \tag{5}$$

Due to small variations in silicon wafer process, the silicon wafer and process for introducing defects change as a result of image sensor amplifier optical response nonuniformity. Response uniformity including illumination and without illumination (DIM) are two environmental conditions. CMOS image sensor for each pixel in both open-loop amplifier, small changes in device manufacturing process lead to bias and gain amplifier to generate substantial differences, and with the further narrow the difference pixel size, further expand, make in the light and in response to a CMOS image sensor two conditions in dark environment uniformity than CCD has a larger gap.

The high quality image sensor collected data into a standard YUV format, to the back processor, processor to complete the compression of video, and through the wired or wireless networks, the compressed video stream is sent. Because the application of environmental monitoring system of relatively large differences, but are in all-weather working state, so the sensor requires very high dynamic range, for example, the sensitivity of the sensor, temperature characteristics, are much higher than ordinary sensor.

Image sensor is using CMOS image sensor OV7670. It has the advantages of small size, low operating voltage, provides all the functionality of monolithic VGA camera and image processor. Controlled via the SCCB bus, can various resolution output frames, subsampling, take the window way of data 8. The product VGA images up to 30 frames per second. The user can fully control the image quality, the data format and transmission.

3. Using FPGA in High-speed CMOS Color Recognition System

Color recognition is applied more and more widely. Widely used in various fields to demand color recognition technology has made considerable development, in combination with other techniques, for industrial control, product manufacturing and other industries to better service. At present, the color recognition technology is mainly realized by simple structure, convenient use of single-chip microcomputer, this design uses FPGA to realize, the system can be used in printing and dyeing, paint, automotive and other industries, can also be installed in the automatic production line to monitor the product color.

In order to get good quality images, carries on processing to the original image data acquisition. In general, the image preprocessing is completed in the coprocessor. Recently, with the development of SoC technology, can be in the CMOS sensor integrated the function of image preprocessing. It just shows the location of CMOS image sensor. The image preprocessing mainly includes a defect correction, remove the FPN noise, color difference, the difference image sharpening, aperture correction, Gamma correction and a series of processing.

The main function of the sequential part is to drive the CMOS image sensor to work, drive timing requirement makes the design of driving circuit of large scale, high complexity, it is difficult to use the traditional way of describing, must use the description method of higher level, design and implementation of a top-down, so it can be combined with VHDL language and FPGA devices, design the key is to describe the configuration timing relationship between SCCB with VHDL language. According to the top-down design method, to determine the input and output signal, at the same time according to the timing analysis function module, then put all the input and output signals assigned to each function module, each function modules are VHDL design input, function simulation, simulation.

The core parts of the design of the digital part, system construction are based on the NiosII processor. A voltage signal after filtering, is transferred to the A / D converter, the A / D conversion by digital signal, prepare for the digital part recognition of signal processing. According to the working principle of the selection of the color sensor, using SOPC control system, the 3 analog circuit signal to enhance the system accuracy of A / D conversion synchronization. In the premise of ensuring the reliability and precision, in order to reduce the system cost, meet the input digital signal ratio requirements, A / D converter using 8 bit serial output ADC0809 converter [8]. Using the Nicosia soft is to build the FPGA system for processing digital signal.

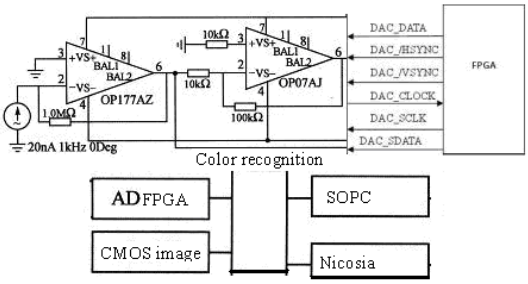

Fig. 2. The design of using FPGA in High-speed CMOS Color Recognition System

SCCB is a simplified I2C protocol, SIO-l is the serial clock input line, the SIO-O is a serial bidirectional data lines, and SCL and SDA is equivalent to I2C protocol respectively. Bus timing and I2C SCCB is basically the same as the ACK response signal, it is called a transmission unit ninth, divided into NA. Don't care produced by the machine; NA produced by the host, because the SCCB does not support multiple byte read and write, NA must be high level. In addition, the concept of SCCB is not repeated start, therefore in the read cycle of SCCB, when a host sends the on-chip register address, must send a bus stop condition. Otherwise, in sending a read command, the machine will not be able to generate don't care response signal.

This design uses the VHDL hardware description language, according to the top-down design method, the sequential control part is divided into three modules: the reset module, register configuration module and the shutter module. The register has two kinds of configuration mode, shutter mode also has two, so after the two part can be subdivided into two small modules. It has strict relation of three major modules, must be in before a module has been completed, only after the start of the module, as is shown by equation 6.

$$X' = W(X,P) = \begin{pmatrix} a_1 & a_2 & d_1 \\ a_3 & a_4 & d_2 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} x \\ y \\ 1 \end{pmatrix} \tag{6}$$

Power CMOS integrated circuit is very low, internal heating is less, but, CMOS circuit structure and electrical parameters have symmetry, the temperature of the environment changes, some parameters can play a role of automatic compensation, so the temperature characteristics of CMOS integrated circuit is very good. Circuit of general ceramic metal package, the working temperature is -55 ~ +125 □; circuit operating temperature range of plastic package is -45 ~ +85 □.

Since the input impedance of the CMOS integrated circuit and high output swing, so easy to be driven by other circuit, also easy to drive circuit or device of other types of. Set the OV7670 frame through the SCCB bus, power system need to initialize the CMOS image sensor, to determine the image window, window size and position of black and white working mode. These parameters are affected by the internal OV7670 the value of the corresponding register control, can be set via the SCCB bus. SCCB interface has a SCCE, SIO_C, SIO_D (SCCE is the serial bus enable signal, SIO_C is a serial bus clock signal, SIO_D is a serial data signal) three pin [9]. No SCCE pin of the OV7670 chip, but also can realize single from the way of communication.

$$P_{j-1} f = P_j f + Q_j f = \sum_k c_k^j \phi_{jk} + \sum_k d_k^j \psi_{jk} \tag{7}$$

The image data of the system input is through the OV6620 collection in; programmable device CPLD using Altera's EPM7128S, the program was written in QuartusII using Verilog hardware programming language; as the system's data buffer, SRAM uses the IS61LV5128, provides the convenience of the random access procedure for image processing; LPC2214 PLL (phase-locked loop) support the highest can run at a frequency of 60 MHz, provides hardware support for fast image processing.

High sensitivity for low light applications; low voltage suitable for embedded application; a standard SCCB interface, compatible with I2C interface; RawRGB, RG (GRB4:2:2, RGB565/555/444), YUV (4:2:2) and YCbCr (4:2:2) output format; support for VGA, CIF, and from CIF to various dimensions of 40x30; Vario Pixel automatic sampling method; effect of the control functions include: automatic exposure control, automatic gain control, automatic white balance, automatic elimination of light stripe, automatic black level calibration. Image quality

control includes color saturation, hue, gamma, sharpness and ANTI_BLOOM; ISP can eliminate the noise and the dead pixel compensation function; support flash: LED lamp and xenon lamp; support the image zoom lens; light loss compensation; 50/60Hz detection; saturation automatic regulation (UV); edge enhancement automatic adjustment; noise automatically.

Because the FPGA chip RAM internal resources Co., video data cannot be stored too much and its treatment, so during the design of the system, plus two SRAM chips to assist FPGA video signal acquisition. Two pieces of SRAM can carry 16 bits of data storage, so that the OV7670 can be configured as an 8 or 16 bit data mode of operation, improve the flexibility of the system.

4. Application of FPGA in High-speed CMOS Digital Image Acquisition and Color Recognition System

Timing in order to produce the required system, using field programmable gate array (FPGA), FPGA includes programmable logic macro cells, programmable I/ O unit, programmable interconnect three kinds of structure, the degree of integration is much higher than that of PAL, GAL, EPLD and other programmable device, and has certain advantages in speed. It is a special integrated circuits (ASIC) a semi-custom circuit in the field but appear, solve the lack of custom circuit, and overcome the original programmable gate limited number of faults.

With the new technology, new materials continue to emerge, in the modern industry, more and more applications of color recognition system, is more complex. By the color sensor as the detector, FPGA uses NiosII embedded soft-core processor as the color recognition system operation, the control of the core, has the advantages of simple structure, high reliability, convenient use, scalability. The processing function of FPGA fast and powerful, can realize the fast, accurate color recognition. The use of modern information fusion technology, using the color sensor model, high sensitivity, fast response, can make the color recognition more accurate, more reliable, as is shown by equation8.

$$\begin{aligned} Z(l) &= \{Z(l,1), Z(l,2), \cdots, Z(l,M)\} \\ &= \{Z_1(l), Z_2(l), \cdots, Z_{N_0}(l)\} \end{aligned} \tag{8}$$

Shai Min sensor is responsible for the different color light signals into electrical signals, but the current signal is only tens to hundreds of nA orders of magnitude, need amplifying circuit to amplify the required degree. The weak current signal is transmitted to the corresponding line channels of different colors produced, through the following 3 stage amplifier, current signal nA is converted to a voltage signal V.

CMOS integrated circuit logic high level "1", "0" low logic level are close to a power supply high voltage and low potential of VSS VDD film. When VDD=15V, VSS=0V, output logic swing approximate 15V. Therefore, voltage integrated circuits using CMOS coefficients in various types of integrated circuit index is higher. Typical voltage noise of the MOS integrated circuit tolerance value is 45% of the supply voltage; ensure the value is 30% of the supply voltage. With the increase of the absolute value of the supply voltage, noise tolerance voltage will increase in proportion. The power supply voltage of VDD=15V (as VSS=0V), the circuit will have noise about 7V tolerance.

This system adopts three-phase write data, namely to send OV7670 address in the ID write register process, then the destination register address to send data, then to write data. If the write data to the serial register, write a register, OV7670 will automatically register address plus 1, the program can continue to write down, and do not need to enter the address again, thus the three-phase write data to two-phase write data, the system only needs to have a discontinuous change limit register data, if you use to configure the methods of all registers, can waste a lot of time and resources, so we only need to change the data in the register to write data. For every change in the register, methods using three-phase write data.

Sensor technology of image sensor application of unique, by reducing or eliminating the optical or electronic defects such as fixed pattern noise, trailing, float, improve the quality of the image, the color image is clear and stable. Image acquisition card is the image of the common input device, a slot usually occupied by PC bus. It mainly includes image memory unit, CMOS camera interface, PC bus interface. This paper puts forward a suitable for embedded system design of digital image acquisition module, image data acquisition, "Ping-Pong" mode image cache data, image data acquisition module external interface, and ensure high speed and continuous image acquisition.

The system builds a NiosII processor system in FPGA chip, including NiosIICPU core, is connected with the CPU configurable on-chip device and memory, connected and off-chip device and memory interface, selected representative of red, green, blue 3 colors, respectively, with the corresponding LED color to represent. The color

recognition system has adequate light, convenient detection Based on the interface of CMOS image sensor system FPGA as shown in figure 3. By linking to the input signal, the output signal, the data bus and address bus, the FPGA can control the image sensor, and a SRAM data cache.

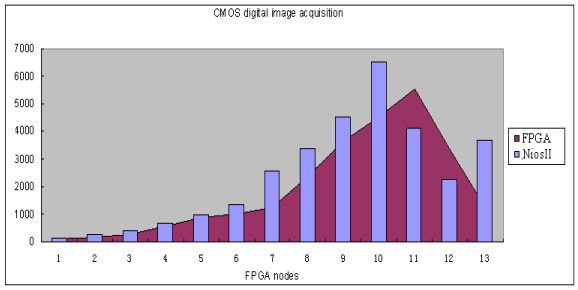

Fig. 3. Comparison results of CMOS digital image acquisition and color recognition system FPGA with NiosII

This paper analyzes the internal logic design of image acquisition and display system based on FPGA, and image processing algorithms such as median filtering, edge detection, image, and picture format. This paper introduces the FPGA control every step of SDRAM read and writes operation image access, research on the I2C bus and image preprocessing algorithm FPGA implementation. The paper presents application of FPGA in high-speed CMOS digital image acquisition and color recognition system.

To improve the comprehensive performance of CMOS image sensor, reduced cell size, adjusting the CMOS parameters, the digital signal processing circuit, image compression, communication circuit are integrated together, and make the filter and micro lens array, in order to achieve low cost, low power consumption, low noise, highly integrated single chip micro imaging system.

CONCLUSION

The system each function module to realize their functions, and then to the top-level design, and designs the VHDL input, functional simulation, synthesis, simulation of the top, until finally reached the design requirements. Image sensor initialization, including setting the image window, frame rate, exposure time etc.. The state machine design based on the part of the program, using the default value, achieve by modifying the different settings to achieve image effect is satisfactory. Build a NiosII processor system in FPGA chip, and it is connected including NiosIICPU core, and CPU configurable on-chip device and memory, connected and off-chip device and memory interface.

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