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Research Article

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A low power broadcast scan scheme

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ABSTRACT

Shift-in power is one of the main elements of the test dynamic power for integrated circuits testing. The paper proposes a low power test scheme for broadcast scan architecture to reduce shift-in dissipation. Unlike conventional broadcast scan, the proposed scheme divides multiple scan chains into several scan chain segments, and only the first internal scan chain is fed directly by the scan Input SI, and used as the path of shifting test data for all the scan chain segments. Thus, only one scan chain is activated when test data shifting in, the test data shift-in power could be reduced effectively. To further reduce test shift-in power, the scan cell reordering which put the similar scan cells in adjacent positions for each two adjacent segments are also used in this paper. The theoretical and the experimental results illustrate that the proposed scheme could reduce dynamic power dissipation during scan testing significantly.

Keywords: low power test, broadcast scan, scan test, scan architecture

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INTRODUCTION

Excessive switching activities often results in too much power being consumed during which often leads to false test failures, or worse, exceeding the power limits of the chip and package, then may causes permanent damage to the chip during test[1].

There are a number of techniques that have been presented in the literature to control power consumption in test mode. Paper [2-3] Proposes new low power testing schemes which using test generation technology for functional broadside test. A new low-power test compression had been proposed for high test quality and low test data volume in paper [4].Selective disabling of the scan chain was proposed in paper [5]. Paper [6] presents a low power testing for SRAMS by reuse of read and write assist circuits. A new test compression scheme based on low power BIST is proposed in paper [7]. Paper[8] presents a low power scan architecture based on Illinois scan that called reference scan. Paper [9] proposes a new scan partition scheme for high test compression ratio and low power.

To reduce test power for the conventional broadcast scan, the paper presents the low power broadcast scan scheme. It divides scan chains into several scan chain segments first, and then putting the similar scan cells in adjacent positions to reduce dynamic power dissipation during test data shift in operation. The theoretical and the experimental results both illustrate the efficiency of the proposed low power scheme.

2. The architecture of the proposed low power broadcast scheme

The simple broadcast architecture is given in the Fig.1. As shown in the figure, as the operation of the ILS architecture, it uses a single scan input to feed all the scan chains in the broadcast scan mode, and the response is collected in a multiple input signature register(MISR) or an Xor compactor. However, unlike the ILS architecture, the scan chain in the low power architecture are divided into m equal length segments of size b(s1,s2…sm as shown in the figure), add a set of multiplexers to route the scan in data to the chains. The first internal scan chain is referred to as the Reference scan chain as paper[8], and it is fed directly by the scan Input SI and contains no multiplexers. All remaining other shared internal scan chains are either fed from the scan block in the same chain or the scan block in Reference scan chain.

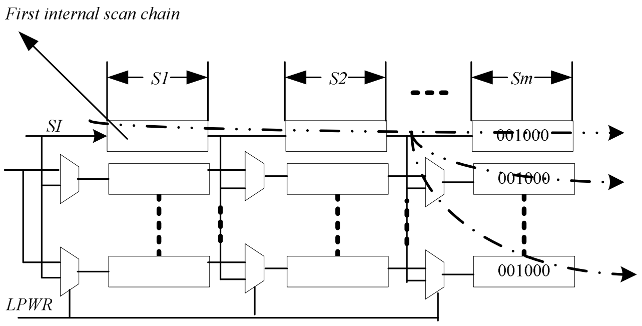


Fig. 1. low power broadcast architecture

During scan-in shift operation, the first internal scan chain is used as a scan-in data cache for the first(n-b) shifts. The other internal scan chain does not receive test data in this operation. For the remaining b shifts, the scan data in the scan segments of the first internal scan chain to shift into the scan segments in the other shared internal scan chain through the multiplexers. The ith scan segment in the shared internal chain receives data from the (i-1)th scan segment in the first internal scan chain. The first scan segment in the shared internal scan receives scan-in data from SI for the last b shifts.

The shift power of the test data of broadcast scan for the scan chain not divided is computed as following (the architecture is given in Fig.2). The same test data are broadcast to all the scan chains that all scan chains have the same shift-in power , the test shift power of each scan chains is denoted as psc in broadcast mode. Thus, the total test data shift in power in this situation is computed as Pn= npsc. However, the low power broadcast architecture uses scan chain partition to reduce shifting power in testing for broadcast mode, and the same data only needs to shifts from the first internal scan chain. It assumes that the test shift in power of the segment j for each scan chain in low power scan architecture is psegj, and the test shift power of segment i for shift test data for segment j is denoted as psegij.

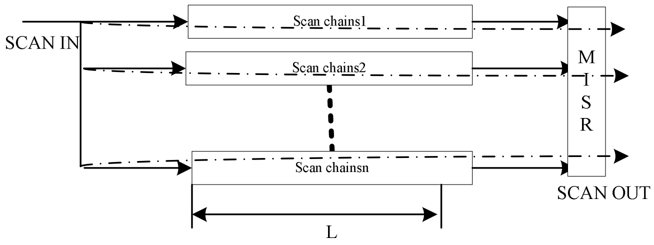


Fig. 2. the broadcast scan without dividing scan chains

As shown in Fig.1, the test shift in power is $n\times p_{segm}+\sum_{i=1}^{m-1}p_{segim}$ for shifting test data to segment m. The total test power for all test data shifted in the scan chain for low power architecture could be computed as pd= $\sum_{j=1}^{m}(n\times p_{segj}+\sum_{i=1}^{j-1}p_{segij})$. The test shift power for Pn is computed in the same way as pn= $\sum_{j=1}^{m}(n\times p_{segj}+n\times\sum_{i=1}^{j-1}p_{segij})$, so the shift in power reduction is given as $p_{reduction}=pn-pd=\sum_{j=1}^{m}(\sum_{i=1}^{j-1}(n-1)p_{segij})$, the detailed presentation matrix of the $p_{reduction}$ is given in Fig.3, as shown in the figure, for the low power scan architecture dividing scan chains into m scan segments, thus, for each segment, test data must not be shifted from all scan chains but only the first internal scan chains, so the shift power is reduced. Take shifting data operation for the segment m for example, for the conventional scan chain, the test data must shifted from all the scan chains, the shift in power is $n\times p_{segm}+n\times\sum_{i=1}^{m-1}p_{segim}$, and now only use the first internal scan chain could the test data shifted into the segment m, the corresponding shift power is $\sum_{j=1}^{m}(n\times p_{segj}+\sum_{i=1}^{j-1}p_{segij})$, so the power reduction is $\sum_{i=1}^{m-1}(n-1)p_{segim}$ which is coincident with the last row of Fig.3.

$$\begin{array}{lllll}
p_{seg12} & & & & \\
p_{seg13} & p_{seg23} & & & \\
p_{seg14} & p_{seg24} & p_{seg34} & & \\
p_{seg15} & p_{seg25} & p_{seg35} & p_{seg45} & \\
\vdots & \vdots & \vdots & \vdots & \\
p_{seg1m} & p_{seg2m} & p_{seg3m} & p_{seg4m} \cdots & p_{seg(m-1)m}
\end{array}$$

Fig. 3. the matrix presentation of the $p_{reduction}$

With m increasing, the variation trend of the $p_{reduction}$ is given in Fig.3, where n=6, as shown in the figure, we could see that the power reduction raise with the number of segments increasing, however, the muxs must be added for each segment which will make the corresponding hardware increase. To further reduce test shift- in power with low hardware cost, the scan chain optimization using scan cell reorder is also proposed in the paper.

3. Test shift-in power reduction using scan cell reordering

The generation of the test shift-in power is because the switching activity that defined as the total number of switch from 0 to 1 or switch from 1 to 0 in each segment, so by putting same test data together could reduce the activity of flip-flops, and thus reduces test power efficaciously. We modify the scan chain cells by scan cells reordering, and the routing length reduced by sorting scan cells only for the adjacent segments under routing constraints.

For every two adjacent segments, the corresponding scan cells are classified to three types scan cells as in paper[10]: 0-dominating scan cells if Ci, 0>Ci, 1, 1-dominating scan cells if Ci, 0<Ci, 1, balanced cells if Ci, 0=Ci, 1, where Ci, 0 and Ci, 1 are the number of 0's and the number of 1's in this cell for the completed test vectors. 0-dominating cells should belong to Chain-0, and 1-dominating cells are designated to chain-1. Balanced cells can be assigned to either chain according to the requirement of other optimization goals. An example is given in Fig.4 in which a test set of six vectors is applied to a can chain consisting of eight scan cells. For scan cells 1, 2, and 8, there are more 0's than 1's in the test set, and thus, they are assigned to the 0-dominant part. However, the scan cells of 3, 4, 5, the 1's more than 0's, so put them into 1-dominant part. The number of 0's and 1's in Scan cells 6 and 7 are equal, so they could be either put into 0-dominant part or put into 1-dominant part.

Weighted Switching activity is one of the important reasons for testing energy. For a cell in a scan chain, the number of switching activity is usually used to measure the energy in testing process, and most of these switching activities are generated by the test data shifting-in operation. The number of test data shifting-in activity is used here to measure the test power. It computed as $SA = \sum_{j=1}^{L-1} (t_{i,j} + t_{i,j+1}) \times j$, where L is the length of the scan chain, $t_{i,j}$ is the jth bit of the test vector t_i.

Fig.5 gives an example of the proposed scheme. The conventional broadcast architecture、the low power broadcast scan architecture and the low power broadcast scan architecture with scan cell reodering are all given in the figure. Consider the test pattern in the figure, which is to be encoded in a fanout-based broadcast scan architecture. The conventional broadcast is given in Fig5.a, the scan architecture is composed of 4 scan chains with 24 cells each, and all shared scan chains receive test data from external chain simultaneously, which is presented by black line in the figure. To use the low power broadcast scan technique, each scan chain is divided into 4 segments, each has six scan cells: S11-S16, S21-S26, S31-S36. The scan-in data flow is illustrated by the red line in the Fig.5.b. The low power broadcast scan architecture with scan cell reordering's is given in Fig.5.c. Scan cells modification for each two adjacent segments were made for reduce shift power in segments with low routing cost. For the first two segments, the scan cells of S26, S12, S15, S16, S22, S24 are 1-dominating cells, and the other scan cells are 0-dominating cells. The second two segments are modified in the same manner. The scan chains after modification are shown in Fig.5.c.

Scan cell	1	2	3	4	5	6	7	8
t1	1	0	x	1	x	x	x	0
t2	x	x	1	1	0	0	x	0
t3	0	0	x	x	x	1	1	1
t4	0	x	x	0	1	0	x	x
t5	x	0	1	x	1	1	0	x
t6	x	1	0	1	1	x	x	0

0-dominating 1-dominating

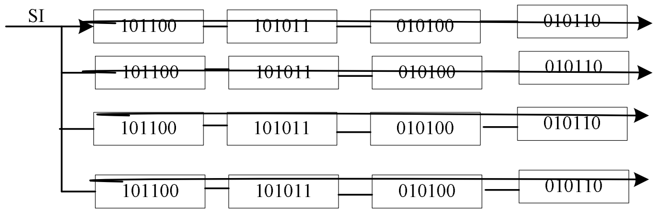
Scan cell	1	2	6	8	3	4	5	7
t1	1	0	x	0	x	1	x	x
t2	x	x	0	0	1	1	0	x
t3	0	0	1	1	x	x	x	1
t4	0	x	0	x	x	0	1	x
t5	x	0	1	x	1	x	1	0
t6	x	1	x	0	0	1	1	x

Fig. 4. modify two adjacent segment

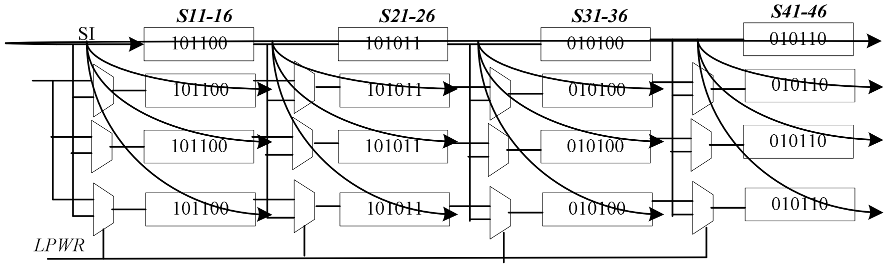
As shown in Fig.5, for the same test patterns, the total WSA(weight switching activity) for the conventional broadcast scan that broadcast same test data to all shared scan chains is 724. The total SA for low power broadcast scan is 602. For low power broadcast scan with scan cell reordering, the total SA is 92. Compared with conventional broadcast scan ,the proposed scheme enormously reduces scan-in shift power.

EXPERIMENTAL SECTION

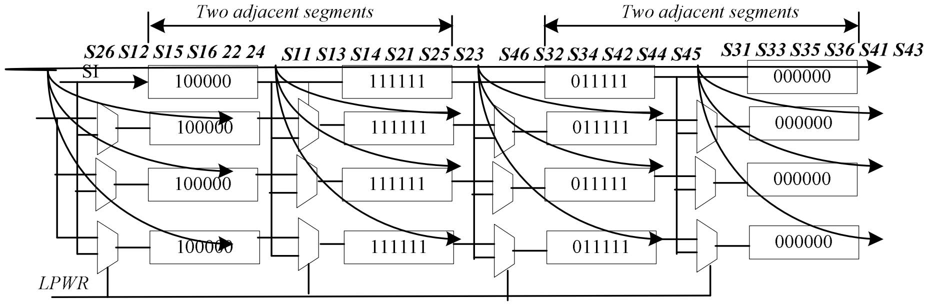
The experiments were carried out on the big ISCAS’89 benchmarks. Test power is measured by switching activity for scan-in shift. The scan-in shift activity is computed for the conventional broadcast scan, low power broadcast architecture and low power broadcast with scan cell reordering. Experimental results are given in table I.



(a) Conventional broadcast scan Total SA=724



(b) Low power broadcast scan Total SA=306



(c) Low power broadcast scan with scan cell reordering Total SA=92

Fig.5 The SA comparison example of the proposed scheme and conventional broadcast scan

Table 1. Proposed scheme compression ratio

circuit	FF	shared sc	Conventional broadcast scan average power(*CBA*)	Low power broadcast scan		Low power broadcast scan with scan cell reordering	
				Average power(*LAP*)	*Sl*	Average power(*LAPR*)	*Slc*
S5378	179	4	6640	2910	53.33	2095	64.40
S9234	211	6	11851	4215	64.43	2276	80.79
S13207	638	8	61104	13515	77.88	6622	89.16
S15850	534	16	34750	10098	70.94	6159	82.27
S38417	1728	16	386314	54827	85.81	38927	89.92
S38584	1426	90	208220	32386	84.45	20727	90.04
average	---	---	----	----	72.81	-----	83.10

RESULTS AND DISCUSSION

As shown in table I, the first and the column presents the circuits and the number of the flip-flops. The third column is the scan chains contained. The conventional broadcast scan's average power that denoted CBA is given in the fourth column. The average power LAP and the average power reduction Sl of the low power broadcast scan are given in the fifth and the sixth column, respectively. The last two columns present the average power LAPR and the low power broadcast scan reduction Slc of the low power broadcast scan with scan cell reordering. Sl and Slc are the power saving ratio compared with conventional low power scan, and they are computed as (CBA-LAP)/CBA, (CBA- LAPR)/CBA, respectively. As illustrated in the table, the proposed low power scan achieve lower test power. This is due to the fact that the proposed method considering shift power in each segment and putting similar scan cells in adjacent positions for each two adjacent segments which induces scan-in switching activity.

The low power scan with scan cell reordering may result in a small longer routing length. However, the proposed technique only makes modification for the adjacent two segments, so the routing length would not be very long. In addition, it only reduces switching activity due to scan-in vector but not consider the other test dissipation power.

CONCLUSION

To reduce power dissipation and test data volume for conventional broadcast scan, the paper proposes a new low power broadcast scan which divides scan chains into several scan chain segments, and then putting the similar scan cells in adjacent positions to reduce dynamic power dissipation during test data shift in operation. The theoretical and the experimental results both illustrate the efficiency of the proposed low power scheme.

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